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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,196	10/30/2001	Hiep P. Ngo	SMQ-067/P5716	4366

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,196	NGO ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,12,13,16,17,28,29 and 32* is/are rejected.

7)☒ Claim(s) *7-11,14,15,18-27,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-32 are pending in the instant application.

Drawings

2. The drawings are objected to because some reference numbers are not plainly legible. The drawings should be replaced with corrected drawings having clearly and easily legible reference numbers.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first receiver stage and the second receiver stage *of the first and second receivers* (fig. 2, refs. 23A and 23B) (claim 4) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. As illustrated, the first and second receivers (fig. 2, refs. 23A and 23B) do not each comprise first and second stages as claimed in claim 4. The first and second stages (fig. 2, refs. 20 and 22, respectively) illustrated can not be considered to be the first and second receiver stages because they do not receive, *respectively*, the clock and data signals as limited by claim 3.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the integration amplifier of the second stage of the first receiver as well as the integration amplifier of the second stage of the second receiver must be shown as claimed in claim 6 or the feature(s) canceled from the claim(s). No new matter should be entered. As illustrated, one integration amplifier is shown (fig. 2, ref. 56) although the claim is most clearly

interpreted to provide for two integration circuits. One of the drawings or the claims must be amended such that the drawings and the claims correspond.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the delay locked loop circuit must be shown as claimed in claim 14 or the feature(s) canceled from the claim(s). No new matter should be entered. As illustrated, a phase locked loop is utilized but a delay locked loop is not illustrated. One of the drawings or the claims must be amended such that the drawings and the claims correspond.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claims 1-32 are objected to because of the following informalities:

Regarding claim 1, in line 3, "correcting timing alignment" should be replaced by –correcting a timing alignment—to provide proper antecedent basis for dependent claims.

Regarding claim 7, in line 2, "of propagation" should be replaced by –of a propagation--, in line 4, "of propagation" should be replaced by –of a propagation--, in line 9, "a output" should be replaced by –an output--, and, in lines 10-11, "of said propagation delay should be inserted into said first and said second transmission path" should be replaced by –of the propagation delay inserted into said first and said second transmission path should be inserted--.

Regarding claim 8, in line 3, "said propagation delay" should be replaced by –the propagation delay—, in line 5, "inserts said propagation" should be replaced by –inserts the amount of the propagation--, and, in line 6, "said input signal asserted" should be replaced by –said output signal provided--.

Regarding claim 9, in line 6, "which" should be replaced by –a--.

Regarding claim 11, the claim is objected to because "the output signal" output by the phase locked loop in claim 7 is limited to be generated by the VCO in the claim. However, according to figure 2 of the drawings, the frequency multiplier (44) generates "the output signal". Further, the claim provides for "a time varying signal" output to the

control circuit by the frequency multiplier although it conflicts with "the output signal" output by the phase locked loop to the control circuit defined in claim 7. In line 8, "phase detector" should be replaced by –a phase detector--.

Regarding claim 15, in line 3, "said control voltage" is lacking antecedent basis.

Regarding claim 18, it is suggested by the Examiner that a carriage return is added between "steps of" and "receiving" in line 4.

Regarding claim 22, in line 5, "said source clock signal and said data signal" should be replaced by –said subsequent source clock signal and said subsequent data signal--.

Regarding claim 27, in line 2, "said system" should be replaced by –a system--.

Regarding claim 28, in line 1, "perform timing" should be replaced by –perform a timing--.

Regarding claim 29, in line 6, "said source door signal" should be replaced by –said source clock signal--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 13, the claim is indefinite because one skilled in the art is unable to determine if the first and second integrated circuits comprise one microprocessor collectively or one microprocessor each.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 2, 28, 29 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Christensen (US 6801592).

Regarding claim 1, Christensen discloses a system for synchronous communication between a first integrated circuit and a second integrated circuit (abstract) comprising: a synchronous interconnect structure (fig. 1) for correcting timing alignment of a data signal and a source clock signal (col. 1, lines 1-15; line 53 – col. 2, line 5) between said first integrated circuit and said second integrated circuit each time said data signal and said source clock signal are transmitted across said synchronous interconnect structure. Christensen discloses by figure 1 a receiver or second integrated circuit of a synchronous communication system. A transmitter or a first integrated circuit of the synchronous communications system is disclosed as generating the synchronous signals D_{in} and Ck_{ref} to the second integrated circuit over a transmission link although it is not shown in the drawings (col. 5, lines 34-38). As broadly as claimed, the first and second circuits (fig. 1) are considered to be "integrated" circuits because the components of the circuits are integrated to work together in an

integrated fashion. Christensen discloses that the second integrated circuit corrects a timing alignment of a data signal D_{in} and a source clock signal Ck_{ref} (col. 5, line 44 – col. 6, line 25). The correction of the timing alignment is performed each time the signals are transmitted between the first and second circuits because the internal clock unit (fig. 1, ref. 51) of Christensen is updated continuously by the source clock signal Ck_{ref} as understood by one having skill in the art and the internal clock is utilized to synchronize the data signal to the source clock signal.

Regarding claim 2, Christensen discloses the limitations of claim 1 as applied above. Christensen further discloses that said synchronous interconnect structure comprises, a deskewing circuit (fig. 1, refs. 6-13; col. 5, line 44 – col. 6, line 25) for connecting said timing alignment between said data signal and said source clock signal.

Regarding claim 28, Christensen discloses a by figure 1 deskewing circuit to perform timing alignment of a synchronous point-to-point signal on a per signal basis comprising (abstract), a control circuit (fig. 1, refs. 3 and 11) to control said timing alignment of said synchronous point-to-point signal (D_{in} and Ck_{ref}); and a phase locked loop circuit (ref. 51) to synchronize said timing alignment of said synchronous point-to-point signal within said control circuit. Christensen discloses that the second integrated circuit corrects a timing alignment of a data signal D_{in} and a clock signal Ck_{ref} (col. 5, line 44 – col. 6, line 25). The correction of the timing alignment is performed each time the signals are transmitted between the first and second circuits because the internal clock unit (fig. 1, ref. 51) of Christensen is updated continuously by the source clock

signal Ck_{ref} as understood by one having skill in the art and the internal clock is utilized to synchronize the data signal to the source clock signal.

Regarding claim 29, Christensen discloses the limitations of claim 28 as applied above. Further, said control circuit comprises, a detection circuit (fig. 1, refs. 11) to detect a phase differential between a first data signal (D_{in}) of said synchronous point-to-point signal and a source clock-signal (Ck_{int}) of said synchronous point-to point signal; and a delay circuit (fig. 1, ref. 3) to perform said timing alignment of said first data signal and said source door signal based on, at least in part, an output signal (fig. 1, ref. 12) of said detection circuit.

Regarding claim 32, Christensen discloses the limitations of claim 28 as applied above. Further, Christensen discloses that the phase locked loop circuit (fig. 1, ref. 51) synchronizes said timing alignment by asserting a time dependent signal (fig. 1, output of reference 10) aligned to said source clock signal to synchronize operation of said delay circuit.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christensen in view of Notani et al (US 6396888; hereafter "Notani").

Regarding claim 3, Christensen discloses the limitations of claim 1 as applied above. Further, Christensen discloses that said synchronous interconnect structure further comprises: a receiver circuit (fig. 1) comprising a first receiver (fig. 1, ref. 5) and a second receiver (fig. 1, ref. 2) wherein said first receiver receives said source clock signal (Ck_{ref}) asserted by a first transmitter and said second receiver receives said data signal (D_{in}) asserted by a second transmitter; and a first transmission line and a second transmission line. The first and second transmission lines are illustrated in figure 1 as conducting the signals D_{in} and Ck_{ref} to the receiver circuit (second integrated circuit). As noted regarding figure 1 above, Christensen discloses a first integrated circuit being a transmitter circuit although it is not illustrated in the drawings. Christensen does not explicitly disclose that the transmitter circuit is comprising a first transmitter and a second transmitter wherein said first transmitter asserts said source clock signal and said second transmitter asserts said data signal. However, Notani teaches a synchronous communications system (fig. 1) wherein the first integrated circuit or transmitter (30) comprises a first transmitter (34) for data (DA), a second transmitter (33) for clock (CKFP), a first transmission line (54) and a second transmission line (51) wherein said first transmission line interconnects said first transmitter and a first receiver (44) and said second transmission line interconnects said second transmitter and a second receiver (43). That is, Notani teaches by an explicit illustration (fig. 1) the first integrated circuit or transmitter disclosed but not illustrated by Christensen as well as a first transmitter and a second transmitter of the transmitter or first integrated circuit. Notani teaches that the first and second transmitters (fig. 1, refs. 33 and 34) are drivers

(col. 12, lines 45-68). One skilled in the art understands that the driver transmitters (fig. 1, refs. 33 and 34) of Notani complement the receivers (fig. 1, refs. 2 and 5) of Christensen such that communication over the transmission lines are robust. Therefore, it would have been obvious to one having ordinary skill in the art to utilize the explicit teachings of Notani of a transmitter having a first and a second transmitter to complement the first and second receivers of Christensen because the synchronous communications link of Christensen in view of Notani would create a robust digital communications link.

Regarding claim 4, Christensen in view of Notani disclose the limitations of claim 3 as applied above. Further, Christensen illustrates in figure 1 that said first receiver and said second receiver each comprise a first receiver stage (respectively 2 and 5) and a second receiver stage (respectively [3, 11, and 12] and [6-10]).

Regarding claim 5, Christensen in view of Notani disclose the limitations of claim 4 as applied above. Further, Christensen discloses that the first receiver stage (fig. 1, ref. 5) of the first receiver and the first receiver stage (fig. 1, ref. 2) of the second receiver each comprise a signal conditioner or buffer (col. 5, lines 60-63; col. 6, lines 10-15). Further, it is implied that the output of a buffer has a fixed output as understood by one having ordinary skill in the art, and, as broadly as claimed, it is implied that the first receiver stages would both utilize a common voltage or have a common mode voltage.

Regarding claim 6, Christensen in view of Notani disclose the limitations of claim 4 as applied above. Further, Christensen discloses that said receiver (fig. 1) comprises: an integration sense amplifier (fig. 1, ref. 3) to integrate and sense a value of said data

signal after said correction of said timing alignment by said deskewing circuit (col. 6, lines 9-25).

12. Claims 12, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christensen in view of Flora et al (US 4755704; hereafter "Flora").

Regarding claim 12, Christensen discloses the limitations of claim 1 as applied above. Christensen does not disclose that the integrated circuits comprise VLSI integrated circuits. However, VLSI circuits are notoriously known in the art, and one skilled in the art is well aware that VLSI circuits provide the benefits of large circuits applied in a small area having high speed and low power. Flora discloses the use of VLSI circuits in a clock de-skewing circuit (col. 2, lines 35-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the notoriously known integrated circuit implementation of VLSI as disclosed by Flora for the integrated circuits of Christensen because they provide the benefits of large circuits applied in a small area having high speed and low power.

Regarding claim 16, Christensen discloses the limitations of claim 1 as applied above. Christensen discloses the circuits, but does not explicitly disclose that the circuits are mounted to a printed circuit board. The use of printed circuit boards are notoriously known in the art for mounting integrated circuits. Flora illustrates a notoriously known printed circuit board (fig. 1, ref. 2) with various integrated circuits mounted upon it (fig. 1, ref. 5; col. 3, lines 30-68). One skilled in the art would have been motivated to mount an integrated circuit to a printed circuit board as illustrated by Flora because a printed circuit board allows many integrated circuits to communicate

and provide power. Further, as known by one having skill in the art, a printed circuit board can be utilized to provide utility for an integrated circuit by allowing it to be wired into a circuit (i.e. to use it). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to mount the integrated circuit of Christensen to the printed circuit board of Flora because, among other reasons, it would allow the integrated circuit to be connected to other circuits.

Regarding claim 17, Christensen discloses the limitations of claim 1 as applied above. Christensen discloses the first and second circuits, but does not explicitly disclose that the first and second circuits are mounted to first and second printed circuit boards. The use of printed circuit boards are notoriously known in the art for mounting integrated circuits. Flora illustrates notoriously known printed circuit boards (fig. 1, ref. 2) with various integrated circuits mounted upon them (fig. 1, ref. 5; col. 3, lines 30-68). One skilled in the art would have been motivated to mount an integrated circuit to a printed circuit board as illustrated by Flora because a printed circuit board allows many integrated circuits to communicate and provide power. One skilled in the art would find it obvious to mount one integrated circuit to one board and another integrated circuit to another board as illustrated because one printed circuit board may not be large enough to mount a large number of integrated circuits. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to mount the first integrated circuit of Christensen to the first printed circuit board of Flora and the second integrated circuit to the second printed circuit board, because among other reasons, it would allow the integrated circuits to be connected to each other by a

connection between the two printed circuit boards in the case that one circuit board may not accommodate many integrated circuits.

Allowable Subject Matter

13. Claims 7-11, 14, 15, 30, and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims *and amended to over come the claim objections applied above*.

14. Indication of allowable subject matter is made regarding claims 18-27. However, the claims must overcome the claim objections applied above.

15. The following is a statement of reasons for the indication of allowable subject matter:

The indication of allowable subject matter is made over the prior art of record because the prior art of record does not disclose or obviate the use of two delay lines utilized on the receiving side of a synchronous link to adjust the timing of the data and clock signals of the synchronous link individually to create a proper timing alignment between the data and clock signals.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to further show the state of the art with respect to synchronous synchronizers.

U.S. Pat. No. 5539344 to Hatakenaka.

U.S. Pat. No. 6028816 to Takemae et al.

U.S. Pat. No. 6285225 to Chu et al.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
February 23, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER